# Errata Note

# SX1232 - 868 & 915MHz
# High Link Budget Integrated UHF Transceiver

Revision 3 - July 2013

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# 1 Chip Identification

The V2B chips are identified as follows:

1) The *RegVersion* at address 0x42 returns 0x22.
2) The top marking described in Figure 1:

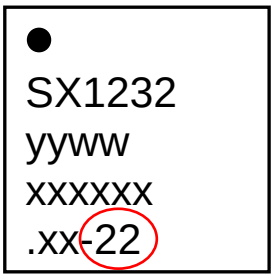


**Figure 1. Chip Marking**

# 2 I and Q Calibration

## *2.1 Description*

By default in the SX1232, I&Q calibration is done at power-up and after a manual reset. In the V2B chip version, the I&Q calibration is not optimal, and the user should manually perform it after a power-on reset or manual reset event, to improve RSSI accuracy and Image Rejection.

## *2.2 Workaround*

This following workaround procedure should be performed once after the power-on of the chip, after Reset if the chip is Reset, and on any user-triggered calibration, initiated with bit *ImageCalStart*, in *RegImageCal*.

1) Go or stay in Standby mode.
2) Use 256 samples for RSSI averaging. To do so, set *RssiSmoothing* to '111' in *RegRssiConfig.*
3) Set *ImageCalStart* to '1' to trigger a manual I&Q calibration.
4) Wait for 8 ms.
5) Set *RssiSmoothing* back to the desired value ('010' by default).

The use of the automatic calibration trigger, based on a pre-defined temperature change threshold, is therefore not recommended. The user can still detect a large temperature variation with the flag *TempChange*, but one should avoid using *AutoImageCalOn* = 1.

### 2.3 SW Implementation

This following pseudo code shows the SW implementation of this workaround:

```
// Rx I&Q re-calibration workaround
RadioWrite( 0x0E, 0x07 );
RadioWrite( 0x3B, 0x43 );

// Wait for 8ms
Sleep( 8 );

// Set RSSI default averaging back to 8 samples
RadioWrite( 0x0E, 0x02 );
```

**Figure 2. SW Implementation**

# 3 *PayloadReady* Set for 31.25ns if FIFO is Empty

## 3.1 Description

When receiving in Packet mode with the SX1232, the microcontroller can be instructed to service the FIFO and read the bytes it contains before the *PayloadReady* flag is set, thanks to the *FifoLevel* gauge. On the SX1232 V2B, the duration of *PayloadReady* is very short (31.25ns) if the FIFO is already emptied at packet end, when this interrupt fires.

This situation can happen if *FifoThreshold* and the corresponding *FifoLevel* interrupts are used to monitor the FIFO content and offload it on-the-go, *FifoThreshold* being equal to the number of bytes stored in the FIFO.

## 3.2 Workaround

When *FifoLevel* interrupt is used to offload the FIFO, the microcontroller should monitor both PayloadReady and *FifoLevel* interrupts, and read only (*FifoThrehold*-1) bytes off the FIFO when *FifoLevel* fires.

# 4 Erroneous IBM Data Whitening/De-Whitening

## 4.1 Description

On the SX1232, the implementation of the IBM-compatible whitening/de-whitening algorithm is erroneous, which makes it incompatible with the standard implementation.

Conditions:

- ✓ *CrcWhiteningType* = 1
- ✓ *DcFree* = 10

## 4.2 Workaround

The workaround is to use “unlimited Length Packet Format”, and process whitening/de-whitening in the host microcontroller. Semtech is providing software implementations of this algorithm. Please contact your Semtech representative for assistance.

# 5 Revision History

| Revision | Date | Description/Changes |
|---|---|---|
| 1 | May 2012 | Initial release |
| 2 | August 2012 | Detail IQ calibration conditions<br>Add erratum on *PayloadReady* interrupt<br>Add erratum on CRC calculation with whitening On and CRC IBM |
| 3 | July 2013 | Correction on IBM whitening description |

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