dsPIC33EPXXGS50X Family Silicon Errata and Data Sheet Clarification

The dsPIC33EPXXGS50X family devices that you have received conform functionally to the current Device Data Sheet (DS70005127**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EPXXGS50X family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on Page 15, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various silicon revisions of the dsPIC33EPXXGS50X family are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		B2	B3
dsPIC33EP16GS502	0x4E01	0x4005	0x4006
dsPIC33EP16GS504	0x4E02		
dsPIC33EP16GS505	0x4E02		
dsPIC33EP16GS506	0x4E03		
dsPIC33EP32GS502	0x4E11		
dsPIC33EP32GS504	0x4E12		
dsPIC33EP32GS505	0x4E12		
dsPIC33EP32GS506	0x4E13		
dsPIC33EP64GS502	0x4E21		
dsPIC33EP64GS504	0x4E22		
dsPIC33EP64GS505	0x4E22		
dsPIC33EP64GS506	0x4E23		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33EPXXGS50X Family Flash Programming Specification"* (DS70005160) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				B2	B3
Auxiliary PLL	APLL Lock	1.	The APLL lock bit is asserted directly after enabling the APLL.	X	X
CPU	`div.sd`	2.	When using the `div.sd` instruction, the Overflow bit is not getting set when an overflow occurs.	X	X
CPU	`DO` Loop	3.	PSV access, including Table Reads or Writes in the last instruction of a `DO` loop, is not allowed.	X	X
—	—	4.	—		
Comparator	EXTREF	5.	The comparator does not function when the external reference is used as the DAC reference voltage.	X	X
I^2C	Slave Mode	6.	Bus data can get corrupted when it matches with one of the slave addresses connected to the bus.	X	X
PWM	PWM Module Enabled	7.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X	X
Input Capture	Cascade Mode	8.	When ICx is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead, increments one cycle after the rollover.	X	X
PWM	Push-Pull Mode	9.	When EIPU = `0`, a period update may produce back-to-back pulses.	X	X
Input Capture	Synchronous Cascade Mode	10.	An even numbered timer does not reset on a source clock rollover in a synchronous cascaded operation.	X	X
Output Compare	PWM Mode	11.	In the scaled down timer source for the output compare module, the first PWM pulse may not appear on the OCx pin.	X	X
Output Compare	Interrupt	12.	Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X
PWM	Redundant/ Push-Pull Output Mode	13.	Changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to 1 PWM clock.	X	X
PWM	Trigger Compare Match	14.	The first PWM/ADC trigger event on a TRIGx/STRIGx match may not occur under certain conditions.	X	X
UART	Break Character Generation	15.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X	X
ADC	ADC Sampling	16.	Under specific conditions, multi-core ADC sampling cross-talk noise might be present.	X	X
PWM	Push-Pull Mode	17.	When EIPU = `1`, Period register writes may produce back-to-back pulses under certain conditions.	X	X
I^2C	Slave Mode	18.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X
I^2C	Slave Receive Mode	19.	The Acknowledge Time Status bit (ACKTIM) is asserted only if Address Hold Enable (AHEN) or Data Hold Enable (DHEN) is enabled.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				B2	B3
PWM	Master Time Base Mode	20.	Changes to the PHASEx register may result in missing dead time.	X	X
ADC	DNL	21.	DNL is out of specification at the mid-code boundary in Single-Ended mode.	X	X
PWM	Center-Aligned Complementary	22.	Dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP mode is disabled.	X	X
ADC	Single-Ended Offset Error	23.	Offset error is out of specification in Single-Ended mode.	X	
CPU	Variable Interrupt Latency	24.	When Variable Interrupt Latency is selected (VAR = 1), an address error trap or incorrect application behavior may occur.	X	X
CPU	Context Switching	25.	When nesting more than one interrupt (without the Alternate Working register set) within the interrupts which are using Alternate Working register sets, there will be an unexpected change in the CCTXI<2:0> bits in the CTXTSTAT register while returning from the highest priority interrupt.	X	X
I^2C	Address Hold	26.	In Slave mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X
I^2C	Data Hold	27.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X	X
SPI	SPI Enable	28.	When SPI is enabled for the first time, there may be a spurious clock on the SCK which causes mismatch between the clock and data lines.	X	X
Comparator	Comparator Output Jitter	29.	The comparator module may generate erroneous triggers/interrupts.	X	X
I/O	5V Tolerant	30.	Limited input current to I/O pins that support 5V operation.	X	X
I/O	Schmitt Trigger	31.	Schmitt Trigger output may produce glitches.	X	X
I^2C	Bus Collisions	32.	In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).	X	X
I^2C	Hold Time	33.	Minimum hold time of 300 ns is not achieved when the data hold time bit (SDAHT) is set.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: Auxiliary PLL

The Auxiliary PLL Lock bit (ACLKCON<14>) is asserted directly after enabling the APLL module (ACLKCON<15>).

Work around

Add a 50 µs delay routine after enabling the APLL lock bit.

Affected Silicon Revisions

B2	B3						
X	X						

2. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

B2	B3						
X	X						

3. Module: CPU

Table Write (`TBLWTL`, `TBLWTH`) instructions cannot be the first or last instruction of a `DO` loop.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

4. Module: —

Silicon errata issue 4 has been corrected and does not apply to the current silicon revision.

Affected Silicon Revisions

B2	B3						

5. Module: Comparator

When the External Voltage Reference bit is enabled (EXTREF = 1) in the CMPxCON<5> register, the dedicated Digital-to-Analog Converter (DAC) will not be connected to the respective analog comparators inverting/negative input terminals.

Work around

Configure the External Reference bit, EXTREF = `0` in the CMPxCON<5> register, to select AV_{DD} as the reference for the respective Digital-to-Analog Converter (DAC).

Affected Silicon Revisions

B2	B3						
X	X						

6. Module: I^2C

In applications with multiple I^2C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

B2	B3						
X	X						

7. Module: PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to first assign pin ownership to the PWM module and then enable it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before the actual switching of the PWM outputs begins. This glitch may cause a momentary turn-on of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Perform the following steps to avoid any glitches from appearing on the PWM outputs at the time of enabling:

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.
2. Assign pin ownership to the GPIO module by configuring the PENH bit (IOCONx<15> = 0) and the PENL bit (IOCONx<14> = 0).
3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT<1:0> bits field in the IOCONx register.
4. Override the PWM outputs by setting the OVRENH bit (IOCONx<9> = 1) and the OVRENL bit (IOCONx<8> = 1).
5. Enable the PWM module by setting the PTEN bit (PTCON<15> = 1).
6. Remove the PWM overrides by making the OVRENH bit (IOCONx<9> = 0) and the OVRENL bit (IOCONx<8> = 0).
7. Ensure a delay of at least one full PWM cycle.
8. Assign pin ownership to the PWM module by setting the PENH bit (IOCONx<15> = 1) and the PENL bit (IOCONx<14> = 1).

The code in Example 1 illustrates the use of this work around.

EXAMPLE 1: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;      // Configure PWM1H/RA4 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors
TRISAbits.TRISA3 = 1;      // Configure PWM1L/RA3 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors

IOCON1bits.PENH = 0;       // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;       // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;     // Configure PWM outputs override state to the desired safe state

IOCON1bits.OVRENH = 1;     // Override PWM1H output
IOCON1bits.OVRENL = 1;     // Override PWM1L output

PTCONbits.PTEN = 1;        // Enable PWM module

IOCON1bits.OVRENH = 0;     // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;     // Remove override for PWM1L output

Delay(x);                  // Introduce a delay greater than one full PWM cycle

IOCON1bits.PENH = 1;       // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;       // Assign pin ownership of PWM1L/RA3 to PWM module
```

Example 1 applies when the PWMLOCK Configuration bit is disabled. If the PWMLOCK bit is enabled, unlock/lock routines are required to write to the IOCONx registers.

Affected Silicon Revisions

B2	B3						
X	X						

8. Module: Input Capture

When the IC is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over, but instead, occurs one cycle after the rollover.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules) form a single 32-bit module. In such a configuration, when ICx counts for a 16-bit value (65535 cycles) and rolls over to 0 during the next clock cycle (65536th cycle), ICy should immediately increment by 1. Instead, the ICy timer remains at 0, and during the next clock cycle (65537th cycle), both ICx and ICy timers increment by 1.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

9. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx<11:10> = 0b10) with the Enable Immediate Period Update bit disabled (PTCON<10> = 0), and when operating in (ITB = 0) Master Time Base mode (PWMCONx<9> = 0), a write to the Period register occurs on the PWMx cycle boundaries. This may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins.

Work around

Work around 1: Ensure that the Enable Immediate Period Update bit (PTCON <10> = 1) is set.

Work around 2: Configure the PWM phase-shift value (PHASEx<15:0>) with a value more than 0x0007.

When multiple PWM generators are configured in Push-Pull mode, configure the PWM phase shift value (PHASEx<15:0>) with a value more than 0x0007 for the respective PWM generators.

Affected Silicon Revisions

B2	B3						
X	X						

10. Module: Input Capture

The even numbered timer does not reset on a source clock rollover in Synchronous Cascaded mode operation.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules), ICy and ICx form a single 32-bit module. In Synchronous Cascaded mode (IC32 = 1, ICTRIG = 0 and the SYNCSEL<4:0> bits are not equal to 0h), both timers, ICyTMR:ICxTMR, must reset on a Sync_trig input from the 32-bit source timers, but only the odd timer (ICxTMR) is getting reset on a Sync Trigger input.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

11. Module: Output Compare

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS<1:0> (TxCON<5:4>).

Work around

- Configure the prescaler for the source timer to 1:1 for output compare.
- The scaled down timer (1:8, 1:64 or 1:256) can be used as a source for the output compare.

Affected Silicon Revisions

B2	B3						
X	X						

12. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM<2:0> = 0b001, 0b010 or 0b100)
- One of the timer modules is being used as the time base
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing the OCM<2:0> bits after the One-Shot mode compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing the OCM<2:0> bits. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

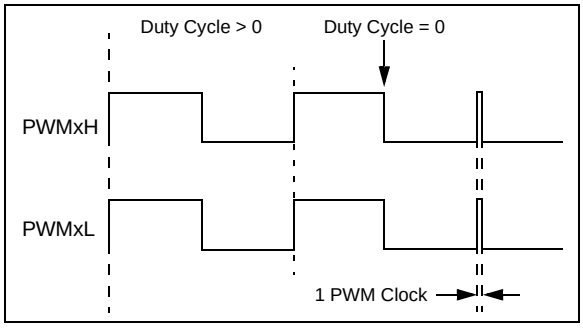
Affected Silicon Revisions

B2	B3						
X	X						

13. Module: PWM

In the Redundant Output mode (IOCONx<11:10> = 0b01) and Push-Pull Output mode (IOCONx<11:10> = 0b10), with the Immediate Update Enable bit disabled (PWMCONx<0> = 0), when the Duty Cycle register is updated from a non-zero value to zero, a glitch pulse of a width equal to 1 PWM clock will appear at the next PWM period boundary, as shown in Figure 1 (for the Redundant Output mode). The Duty Cycle register refers to the PDCx register if PWMCONx<8> = 0 or the MDC register is PWMCONx<8> = 1.

FIGURE 1: EXAMPLE FOR REDUNDANT OUTPUT MODE



Work around

If the application requires a zero duty cycle output, there are two possible work around methods:

1. Use the PWM override feature to override the PWM output to a low state instead of writing to the Duty Cycle register. In order to switch back to a non-zero duty cycle output, turn off the PWM override. The override-on and override-off events must be timed close to the PWM period boundary if the IOCONx register has been configured with IOCONx<0> = 0 (i.e., output overrides through the OVDDAT<1:0> bits occur on the next CPU clock boundary).
2. Enable the Immediate Update Enable bit (PWMCONx<0> = 1) while configuring the PWMx module (i.e., before enabling the PWMx module, PTCON<15> = 1). With the Immediate Update enabled, writes to the Duty Cycle register can have an immediate effect on the PWM output. Therefore, the duty cycle write operations must be timed close to the PWM period boundary in order to avoid distortions in the PWM output.

Affected Silicon Revisions

B2	B3						
X	X						

14. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) and the PWMx Secondary Trigger Compare Value register (STRIGx) will not trigger at the point defined by the TRIGx/STRIGx register values on the first instance for the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx, STRIGx are less than 8 counts
- Trigger Output Divider bits, TRGDIV<3:0> (TRGCONx<15:12>), are greater than '0'
- Trigger Postscaler Start Enable Select bits, TRGSTRT<5:0> (TRGCONx<5:0>), are equal to '0'

Work around

Configure the PWMx Primary Trigger Compare Value Register (TRIGx) and PWMx Secondary Trigger Compare Value Register (STRIGx) values to be equal to or greater than 8.

Affected Silicon Revisions

B2	B3						
X	X						

15. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA<11>), to be cleared instead of the TRMT bit (UxSTA<8>) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

B2	B3						
X	X						

16. Module: ADC

When using multiple ADC cores, if one of the ADC cores completes conversion while other ADC cores are still converting, the data in the ADC cores which are converting may be randomly corrupted.

Work around

Work around 1: When using multiple ADC cores, the ADC triggers are to be sufficiently staggered in time to ensure that the end of conversion of one or more cores doesn't occur during the conversion process of other cores.

Work around 2: For simultaneous conversion requirements, make sure the following conditions are met:

1. All the ADC cores for simultaneous conversion should have the same configurations.
2. Avoid shared ADC core conversion with any of the dedicated ADC cores. They can be sequential.
3. The trigger to initiate ADC conversion should be from the same source and at the same time.

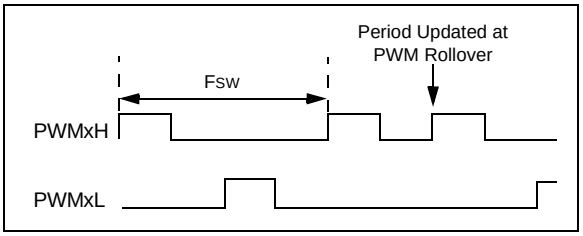
Affected Silicon Revisions

B2	B3						
X	X						

17. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx<11:10> = 0b10) with the Enable Immediate Period Update bit enabled (PTCON <10> = 1), a write to the Period register that coincides with the period rollover event may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins (Figure 2).

FIGURE 2:



Work around

Ensure that the update to the PWM Period register occurs away from the PWM rollover event by setting the EIPU bit (PTCON<10> = 1). Use either the PWM Special Event Trigger (SEVTCMP) or the PWM Primary Trigger (TRIGx) to generate a PWM Interrupt Service Routine (ISR) near the start of the PWM cycle. This ISR will ensure that period writes do not occur near the PWM period rollover event.

Affected Silicon Revisions

B2	B3						
X	X						

18. Module: I²C

In I²C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence. This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes.

The hardware asserts the ACKTIM on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

B2	B3						
X	X						

19. Module: I²C

In I²C Slave Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if Address Hold Enable (AHEN) and Data Hold Enable (DHEN) are disabled (AHEN = 0 and DHEN = 0). The Acknowledge Time Status bit (ACKTIM) is asserted only if Address Hold Enable (AHEN) or Data hold Enable (DHEN) is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for the RBF flag.

Affected Silicon Revisions

B2	B3						
X	X						

20. Module: PWM

In Edge-Aligned PWM mode with Master Time Base (PWMCONx<9> = 0) and Immediate Update disabled (PWMCONx<0> = 0), after enabling the PWMx module (PTCON<15> = 1), changes to the PHASEx register, where PHASEx < DTRx or PHASEx > PDCx, will result in missing dead time at the PWMxH-PWMxL transition that will occur at the next master period boundary.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

21. Module: ADC

When the ADC SAR core is configured to operate in Single-Ended mode, the core's DNL performance may be out of specification at the mid-code boundary.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

22. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled under the following conditions:

- PWMx module is enabled (PTEN = 1)
- SWAP is enabled prior to this event

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

23. Module: ADC

When the ADC SAR core is configured to operate in Single-Ended mode, the core's offset error may be out of specification. The affected revisions have the following offset error specifications.

TABLE 3: ADC SAR CORE OFFSET ERROR

AD24b	EOFF	Offset Error (Dedicated Core)	> 18	39	< 58	LSb	AVSS = 0V, AVDD = 3.3V
		Offset Error (Shared Core)	> 8	25	< 38	LSb	

Work around

None.

Affected Silicon Revisions

B2	B3						
X							

24. Module: CPU

An address error trap or incorrect application behavior may occur if the variable exception processing latency is enabled by setting the VAR bit (CORCON<15> = 1).

Work around

Enable the Fixed Interrupt Latency mode by clearing the VAR bit (CORCON<15> = 0).

Affected Silicon Revisions

B2	B3						
X	X						

25. Module: CPU

When returning from an Interrupt Service Routine (ISR) by executing the RETFIE instruction, in the case of a nested interrupt, the Interrupt Priority Control bits (IPC<3:0>) associated with the lower priority interrupt are compared with the CTXTn bits field in the FLTREG Configuration register:

- If there is a match with either of the CTXTn bits field, then the corresponding Alternate Working Register Set is chosen and the Current Context Identifier bits (CCTXI<2:0>) in the CTXTSTAT register are updated to reflect the new Alternate Working Register Set.
- If there is no match with either of the CTXTn bits field, then the expected behavior is to keep the context (defined by the value of the Current Context Identifier bits, CCTXI<2:0> in the CTXTSTAT register) unchanged. However, the context gets changed. A new context, corresponding to the value in the Manual Context Identifier bits (MCTXI<2:0>) in the CTXTSTAT register, is selected by the hardware and the CCTXI<2:0> bits in the CTXTSTAT register are modified to reflect this change.

When using interrupts with the Alternate Working Register Set (automatic context assignment), no more than one ISR without an Alternate Working Register Set must be nested within an ISR with an Alternate Working Register Set.

Issue and work around are illustrated in Figure 3 and Figure 4, respectively. The figures show the status bits, CCTXI<2:0> and MCTXI<2:0>, after entering into an ISR from a lower priority ISR (left pane), and after returning to the same ISR from a higher priority ISR (right pane).

FIGURE 3: MISMATCH OF WORKING REGISTER SET WHEN NESTING MORE THAN ONE INTERRUPT WITHIN INTERRUPTS THAT USE ALTERNATE WORKING REGISTER SETS

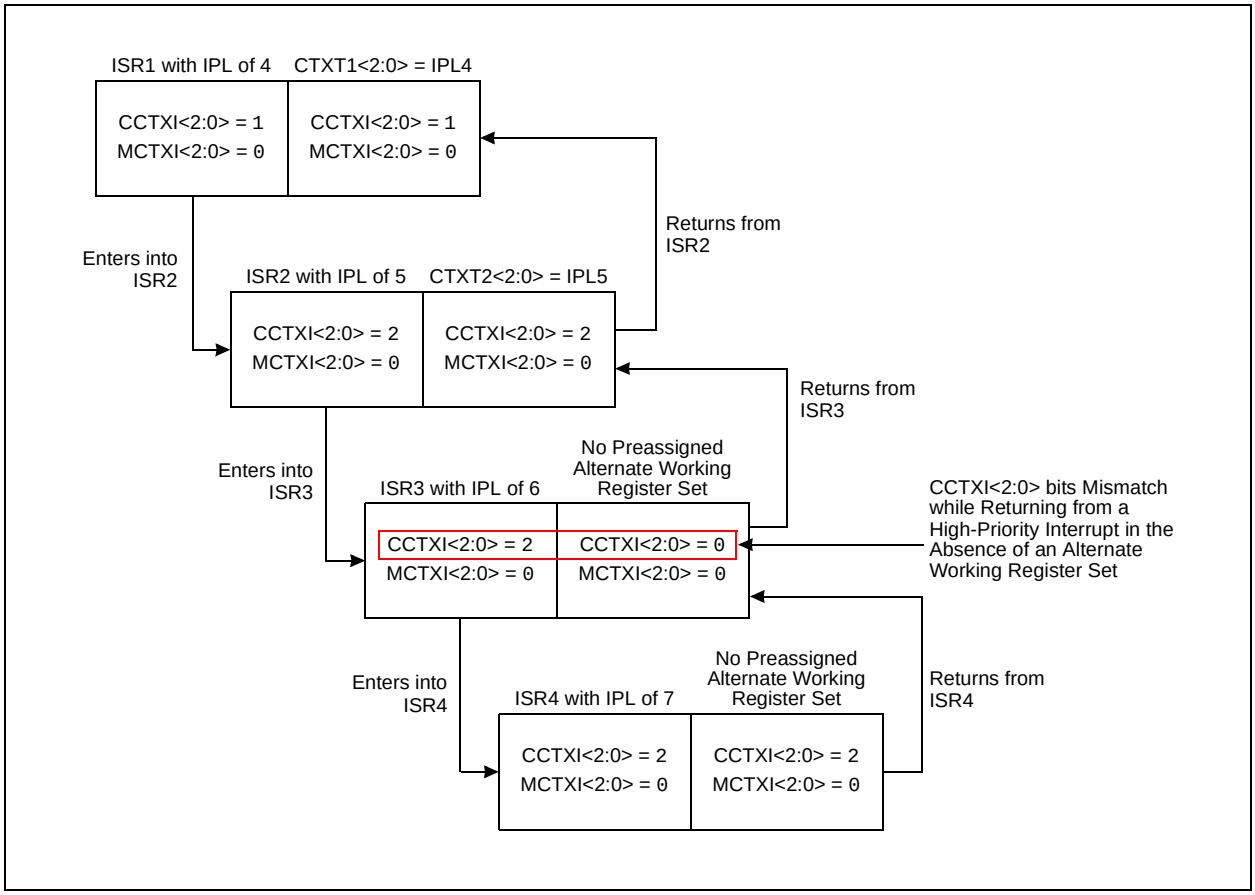
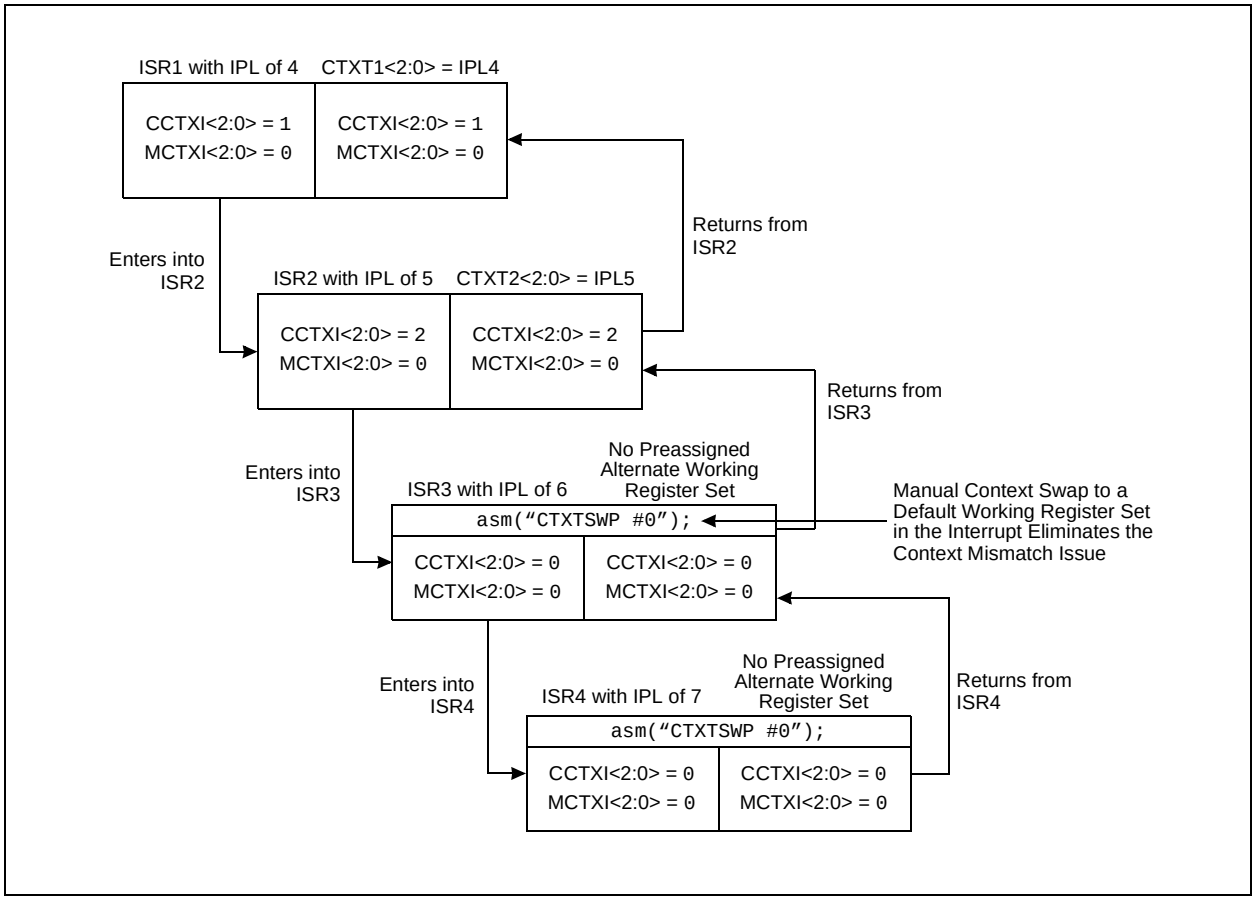


FIGURE 4: WORKAROUND FOR MISMATCH OF WORKING REGISTER SET WHEN NESTING MORE THAN ONE INTERRUPT WITHIN INTERRUPTS THAT USE ALTERNATE WORKING REGISTER SETS



Work around

Work around 1: When using interrupts with the Alternate Working Register Set, at the entry of all ISRs that do not have an Alternate Working Register Set and have a higher IPL level than the ISRs with an Alternate Working Register Set, perform a manual context swap to Context #0 as:

```
asm("CTXTSWP #0");
```

Note: The application software must not perform a manual context swap (using the CTXTSWP instruction) to a context other than Context #0.

Work around 2: Always assign higher IPLs for the ISRs that use an Alternate Working Register Set than for the ISRs that do not use an Alternate Working Register Set.

Affected Silicon Revisions

B2	B3						
X	X						

26. Module: I²C

In Slave mode, when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

B2	B3						
X	X						

27. Module: I²C

In Slave mode, when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

B2	B3						
X	X						

28. Module: SPI

When SPI is enabled for the first time, there may be a spurious clock on the SCK. This may result in one bit of data shifted out on the data line, resulting in a mismatch between the clock and data lines.

This issue may also occur when the SPI is disabled during data transmission and enabled subsequently.

Work around

1. Disable the SPI module after two SPI cycles and then re-enable SPI; this will synchronize the clock and data.
2. If the SPI is configured on PPS pins, first enable the SPI without configuring the PPS, then allow two SPI clocks to pass and then configure the PPS to connect to the SPI module. This will prevent the spurious SPI clock going out on the pin. If the SPI module is turned off periodically, ensure to turn off the PPS as well.

Affected Silicon Revisions

B2	B3						
X	X						

29. Module: Comparator

Analog comparator output may have a jitter when it is operating and this will generate erroneous triggers/interrupts. If the PWM module is configured to be controlled by an analog comparator, the output of the PWM generator may be affected by jitter in the analog comparator output.

Work around

Configure the Comparator Hysteresis Select bits, HYSSEL<1:0>, as '0b11' (20 mV hysteresis) and set the Digital Filter Enable bit, FLTREN (CMPxCON<10>), to '1'.

Affected Silicon Revisions

B2	B3						
X	X						

30. Module: I/O

Undesired pin failure may occur on the RC15, RD0, RD4, RD5, RD10, RD12 and RD15 5V tolerant I/O pins.

Work around

If 5V input operation is desired on I/O pins RC15, RD0, RD4, RD5, RD10, RD12 and RD15, use a current-limiting resistor of at least 1 kOhm.

Affected Silicon Revisions

B2	B3						
X	X						

31. Module: I/O

If the input signal rise or fall time is greater than 300 nS, the I/O Schmitt trigger output may have glitches.

Work around

The rise/fall times must be less than 300 nS.

Affected Silicon Revisions

B2	B3						
X	X						

32. Module: I²C

In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

33. Module: I²C

Minimum hold time of 300 ns on SDAx after the falling edge of SCLx is not achieved when the Data Hold Time bit (SDAHT) is set.

Work around

None.

Affected Silicon Revisions

B2	B3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005127**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ADC

Trigger Source Selection for Corresponding Analog Inputs bits options were stated incorrectly in the data sheet. The correct options are as follows:

bit 4-0 TRGSRC(4x)<4:0>: Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = **PWM Generator 5 current-limit trigger**
11011 = **PWM Generator 4 current-limit trigger**
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = **Output Compare 2 trigger**
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = **PWM Generator 5 secondary trigger**
10010 = **PWM Generator 4 secondary trigger**
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = **PWM Generator 5 primary trigger**
01000 = **PWM Generator 4 primary trigger**
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

2. Module: ADC Module Specifications

In Table 26-43, text is added under the Conditions column for AV_{DD}, which is as follows:

TABLE 26-43: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[5] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AV_{DD}	Module V_{DD} Supply	Greater of: V_{DD} – 0.3 or 3.0	—	Lesser of: V_{DD} + 0.3 or 3.6	V	**The difference between AV_{DD} supply and V_{DD} supply must not exceed ±300 mV at all times, including device power-up**

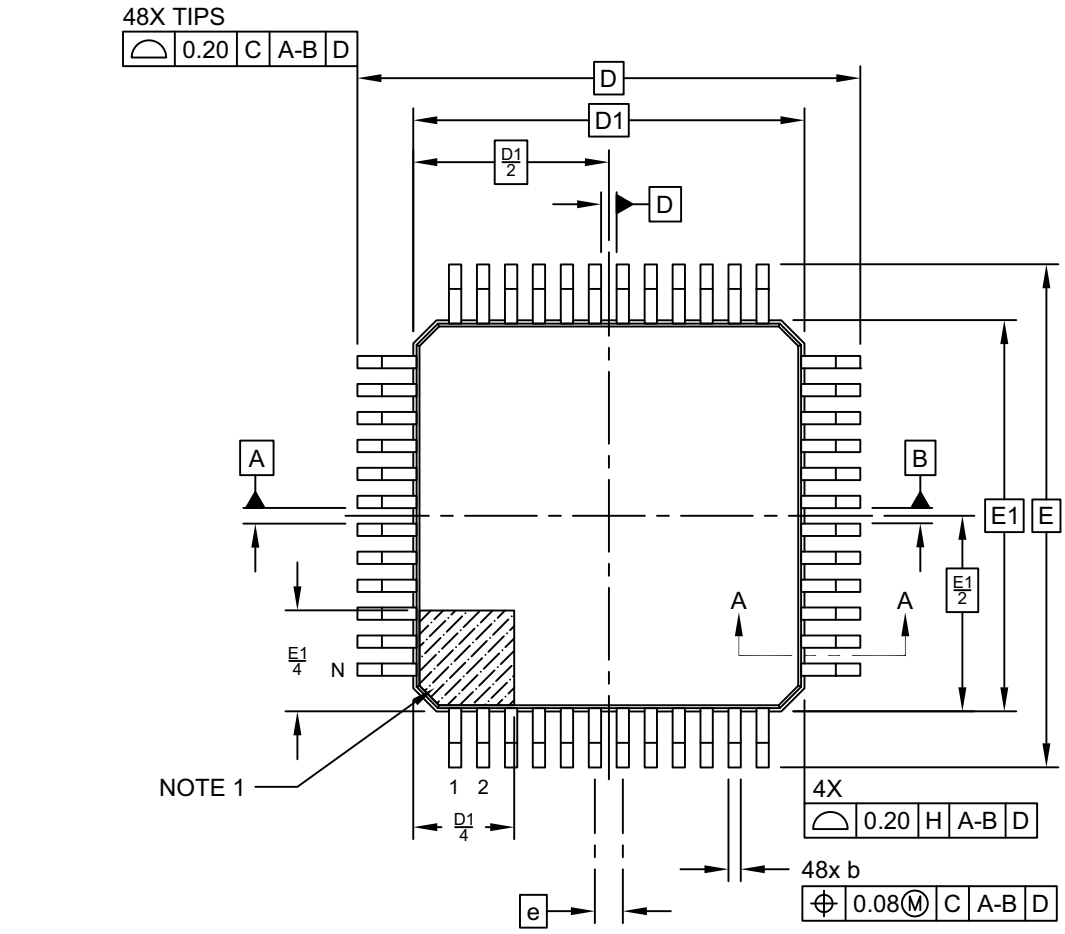
3. Module: Packaging Information

In the *"dsPIC33EPXXGS50X Family Data Sheet"*, **Section 28.2 "Package Details"**, dimensions for the 48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad is mentioned. However, the dsPIC33EPXXGS50X family devices are not available in this package with the exposed pad.

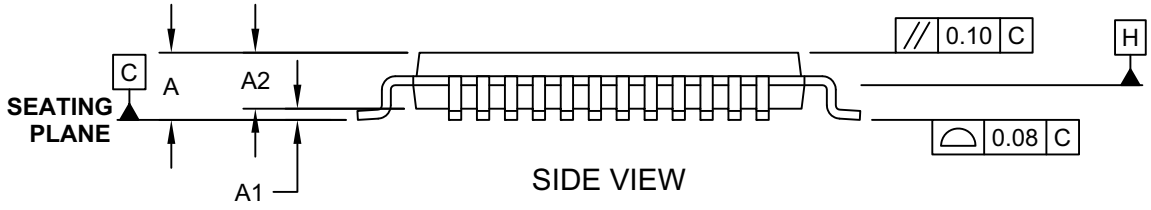
The dsPIC33EPXXGS50X family devices are available in the 48-Lead Thin Quad Flatpack (Y8) - 7x7x1.0 mm Body [TQFP] without Exposed Pad and the package dimensions are shown on the following drawings.

48-Lead Thin Quad Flatpack (Y8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

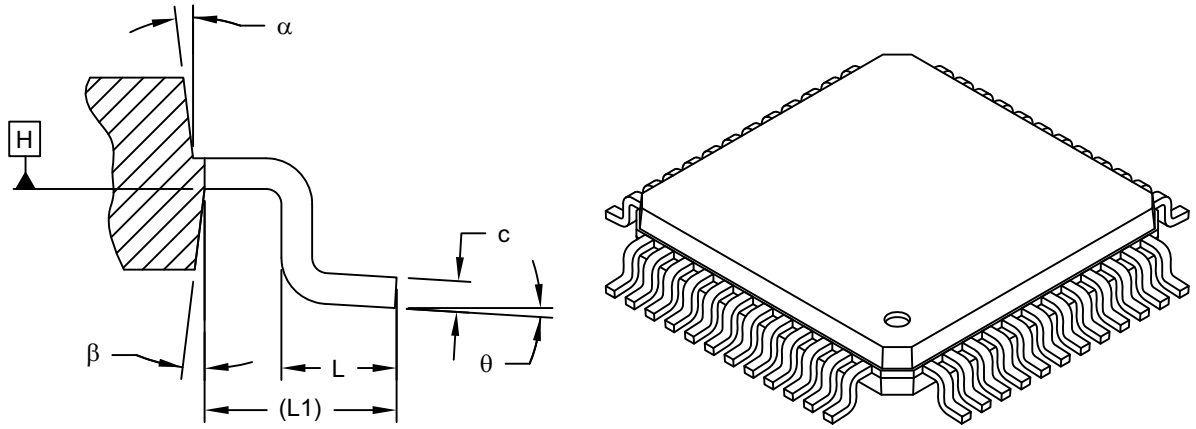


SIDE VIEW

Microchip Technology Drawing C04-300-Y8 Rev A Sheet 1 of 2

48-Lead Thin Quad Flatpack (Y8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

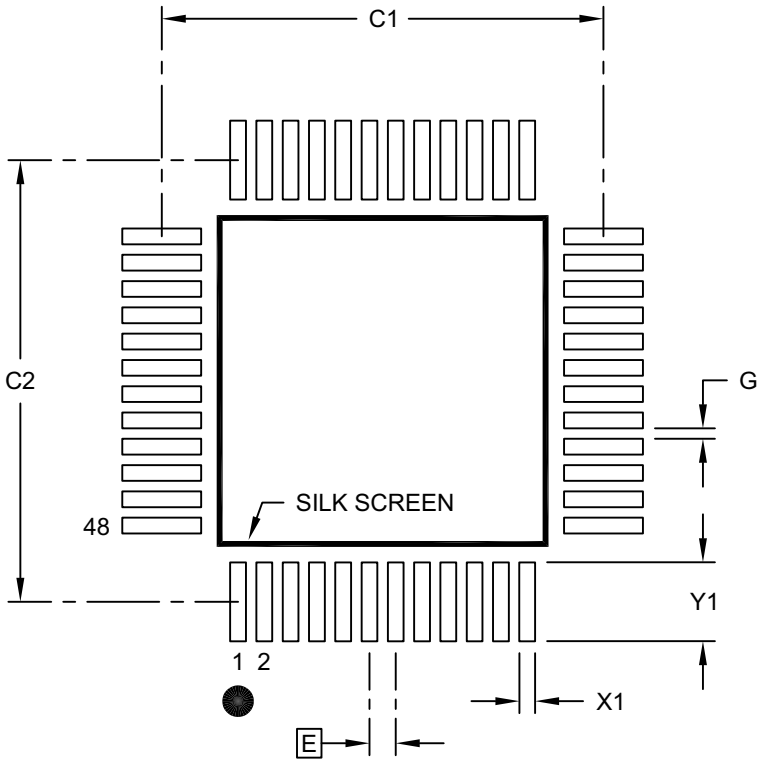
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A-B and D to be determined at center line between leads where leads exit plastic body at datum plane H

Microchip Technology Drawing C04-300-Y8 Rev A Sheet 2 of 2

48-Lead Thin Quad Flatpack (Y8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-Y8 Rev A

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2015)

Initial version of this document; issued for silicon revision B2.

Rev B Document (10/2015)

Adds silicon revision B3.

Adds new silicon issue 23 (ADC).

Rev C Document (3/2016)

Adds new silicon issues 24 (CPU), 25 (CPU), 26 (I^2C), 27 (I^2C), 28 (SPI) and 29 (Comparator).

Adds data sheet clarifications 1 (ADC), 2 (ADC Module Specifications) and 3 (Packaging Information).

Rev D Document (4/2017)

Adds new silicon issues 30 (I/O), 31 (I/O), 32 (I^2C) and 33 (I^2C).

Adds additional text following Example 1 in silicon issue 7 (PWM).

Removes silicon issue 4 (PWM) because the issue with dead time not being asserted when PDCx is updated has been corrected in the current silicon revision.

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